

**REMARKS**

By the present amendment and response, claims 1, 10, 17, 23 and 33 have been amended. Claims 1-35 remain pending in the present application. Applicant respectfully requests reconsideration and allowance of pending claims 1-35 in view of the following remarks.

**A. Rejection of Claims 1, 17, 23 and 33 Under 35 USC §103**

The Examiner has rejected independent claims 1, 17, 23 and 33 under 35 USC §103(a) as being unpatentable over Hollander (US 6,182,258) in view of Chan (US 6,466,898).

By the present amendment, applicant has amended claim 1 to recite: “linking one of said models with another of said models using said set of function calls; executing said virtual prototype, wherein said models communicate through a transaction based interconnect using said set of function calls and cycle accurate information is generated.” It is respectfully submitted that neither Hollander nor Chan discloses, teaches or suggests that the models are linked and communicate through a transaction based interconnect using the set of function calls and cycle accurate information is generated.

Applicant respectfully submits that the Examiner has not made a prima facie as to where and how either Hollander or Chan discloses, teaches or suggests “linking one of said models with another of said models using said set of function calls”, and applicant has not been able to locate any such disclosure. However, to further clarify the invention of claim 1, applicants has amended claim 1 to recite that “said models communicate through a transaction based interconnect using said set of function calls.”

Applicant respectfully submits that Hollander is directed to an improved testbench apparatus and method. Hollander is not directed to the method of claim 1. In fact, Hollander is directed to a technique for generating system tools used to verify a device under test (“DUT”). See, for example, col. 4, lines 44-52 of Hollander. The DUT may be a module, chip, simulation and/or system, and Hollander discloses a testbench, which can be used and re-used to test the DUT. Specifically, Hollander discloses a technique for generating test vectors used as input stimuli to, for example, a simulator. However, Hollander is not directed to the system simulator itself, nor to a method for simulating a system, as specified by claim 1. As such, Hollander neither discloses nor remotely suggests the computer implemented method and/or instructions for simulating a system design, as specified by claim 1. In sum, Hollander is simply directed to a tool for generating a testbench suitable for testing system simulations.

Moreover, as discussed above, claim 1 recites “linking one of said models with another of said models using said set of function calls; executing said virtual prototype, wherein said models communicate through a transaction based interconnect using said set of function calls and cycle accurate information is generated.” Such an approach is neither disclosed nor suggested by Hollander. For these reasons, applicant respectfully submits that the rejection of independent claim 1 has been traversed, and that, therefore, claim 1 should now be allowed.

Furthermore, independent claims 10, 17, 23 and 33 have been amended to recite that the models communicate through a transaction based interconnect using at least one function call and, therefore, claims 10, 17, 23 and 33 should also be allowed.

**B. Rejection of Claims 2-9, 11-16, 18-22, 24-32, and 34-35**

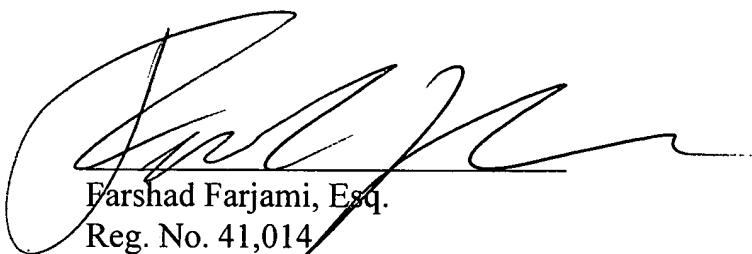
Applicant submits that dependent claims 2-9, 11-16, 18-22, 24-32, and 34-35, being dependent upon allowable base claims, are allowable for the foregoing reasons.

**C. Conclusion**

For all the foregoing reasons, Applicant respectfully requests withdrawal of the final rejection and issuance of a timely Notice of Allowance in the present application.

Respectfully Submitted;  
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